MICROCONTROLLER INPUT/OUTPUT CONNECTOR STATE RETENTION IN LOW-POWER MODES

CLAIM OF PRIORITY

[0001] This application is a continuation of U.S. patent application Ser. No. 14/716,983 filed May 20, 2015, which claims priority to U.S. patent application Ser. No. 13/606,515, filed on Sep. 7, 2012, the entire contents of which are hereby incorporated by reference.

FIELD OF THE DISCLOSURE

[0002] This disclosure relates to retention of the state of microcontroller input/output (I/O) connectors, such as I/O pads and I/O pins, in low-power modes of operation.

BACKGROUND

[0003] Microcontrollers sometimes can operate in various modes, including power savings modes that allow overall power consumption to be reduced. In such low-power consumption modes, power typically is not supplied to some of the modules or components of the microcontroller. However, when the microcontroller enters such a power savings mode, I/O connectors (e.g., I/O pads or pins) for the microcontroller may be in an uncontrolled stated, which can cause undesired complications for other modules or components of the microprocessor, as well as peripheral components that are coupled to the I/O connectors.

SUMMARY

[0004] This disclosure describes retention of the state of microcontroller I/O connectors in a low-power mode of operation.

[0005] For example, in one aspect, a microcontroller is operable in a low-power mode and includes one or more I/O connectors, as well as an I/O controller operable to provide control signals for controlling a state of a particular one of the I/O connectors. The I/O controller is powered off or deactivated during the low-power mode. The microcontroller also includes I/O connector state control logic operable to control the state of the particular one of the I/O connectors in accordance with the control signals from the I/O controller. The I/O connector state control logic includes I/O connector state retention logic that retains states of the control signals and maintains the particular I/O connector in a corresponding state in accordance with the retained control signals while the microcontroller is in the low-power mode.

[0006] Some implementations include one or more of the following features. For example, the I/O connector state retention logic can include latches, each of which is operable to be enabled to latch a respective one of the control signals from the I/O controller. The microcontroller can include a power state manager that provides a signal to cause the latches to latch the respective control signals when the microprocessor enters the low-power mode. When the microprocessor exits the low-power mode, the power state manager releases the signal that caused the latches to latch the respective control signals.

[0007] In some implementations, the control signals from the I/O controller include one or more of: a first signal to drive a logical one or zero onto the particular I/O connector, a second signal to select whether the particular I/O connector is used as an input or an output, and a third signal that selects a drive strength setting.

[0008] According to another aspect, a microcontroller that is operable in a low-power mode includes one or more I/O connectors and an I/O controller operable to provide control signals for controlling a state of a particular one of the I/O connectors. The I/O controller is powered off or deactivated during the low-power mode. The microcontroller includes I/O connector state control logic operable to control the state of the particular one of the I/O connectors in accordance with the control signals from the I/O controller. The I/O connector state control logic includes I/O connector state retention logic that retains respective states of the control signals and maintains the particular I/O connector in a corresponding state in accordance with the retained control signals while the microcontroller is in the low-power mode, thereby executing an I/O connector state retention function. The microcontroller also includes a power state manager, as well as a user interface. Depending on a value stored, for example, in a register, the user interface can be used to facilitate either automated or user-controlled I/O connector state retention. Automated state retention of the I/O connectors can be handled by the power state manager.

[0009] In yet a further aspect, a method of retaining the state of an I/O connector of a microcontroller includes generating, from an I/O controller in the microcontroller, one or more control signals for controlling a state of the I/O connector. The method further includes causing the microcontroller to enter a low-power mode of operation, in which the I/O controller is powered off or deactivated, and storing information indicative of the respective states of the one or more control signals prior to the I/O controller becoming powered off or deactivated. The I/O connector is maintained in a corresponding state in accordance with the stored information while the microcontroller is in the low-power mode.

[0010] The techniques described in this disclosure can facilitate retention of the state of I/O pins, I/O pads and other I/O connectors, even when the microcontroller enters a low-power mode of operation, during which the I/O controller is powered off or deactivated.

[0011] Other aspects, features and advantages will be readily apparent from the following detailed description, the accompanying drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a block diagram showing features of a microcontroller according to some implementations of the invention.

[0013] FIG. **2** illustrates various details of the pad state retention control logic according to some implementations.

[0014] FIG. **3** illustrates portions of the logic for automated control of the pad state retention function.

[0015] FIG. **4** is a timing diagram associated with automated control of the pad state retention function.

[0016] FIG. **5** illustrates portions of the logic for user control of the pad state retention function.

[0017] FIG. **6** is a timing diagram associated with user control of the pad state retention function.

DETAILED DESCRIPTION

[0018] As shown in FIG. **1**, a microcontroller **10**, which can be implemented, for example, as an integrated circuit